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14. ABSTRACT

The technical objective of this research grant was to establish a new discipline that we call ballistic electronics. This means an electronic technology based upon nonlinear ballistic transport and phenomena that exist in nanodevices that have the critical dimension smaller than the carrier mean-free path. Our test devices are structured in 2-dimensional electron gas (2DEG) compound semiconductor heterostructures, thus, can operate our devices in the temperature range up to the room temperature. Our experiments confirmed that our new device called ballistic deflection transistor can operate at several hundreds of gigahertz frequency at room temperature even at transistor channels larger than mena free path. As a second major achievement of this project was that we demonstrated that the BDTs can be integrated into larger circuit blocks performing dedicated functions. This opens the door to larger functionsl integhration inot terahertz speed analog and digital processing. Details of different activities and achievements are presented in the attached files.

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2008-2011 Project Findings: major research findings and results

Our main findings are presented according to the four basic thrusts of our program (see Project Activities):

(a) Design, fabrication, and process optimization (both experimental and modeling) of our ballistic devices. This thrust has been supervised by Profs. Sobolewski and Margala (co-PIs) and executed by Dr. Iniguez (post-docs), and graduate students H. Irie, G. Guarino, and V. Kaushal. Additional assistance was provided by K. Rosario

We have studied experimental dependencies of performance of room temperature BDTs for quasi-ballistic regime, on its dimensional ratios. Experimental transconductance change based on geometry variations was studied for smaller and larger devices with the channel width of 300 nm and 500 nm, respectively. Transconductance variation for a series of drain bias was also observed for a specific geometry and dimension. By means of modeling with Monte Carlo, we reported on the effect of different geometry parameters on the transfer characteristic of ballistic deflection transistors. The strength of the gate control in the InGaAs channel was analyzed.

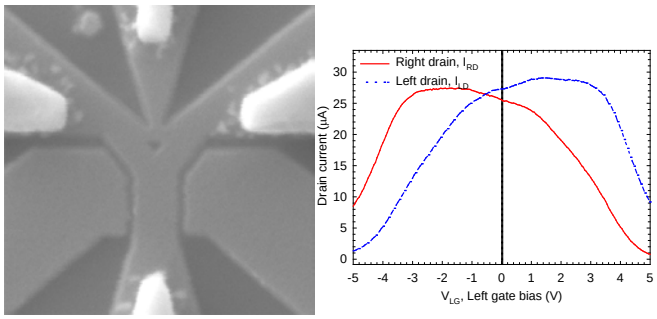


Fig. 1. (a) SEM image (with 500 nm scale indicator) of a BDT with 500 nm channel width and 100 nm gate-channel trench width. The top-left (V_{LD}) and top-right (V_{RD}) ports are drain ports, bottom-left (V_{LG}) and bottom-right (V_{RG}) ports are gates. Top port (V_{TD}) is a bias port that controls gain, and the bottom (V_{SS}) port is the source. Bright regions and dark regions indicate 2DEG and removed material respectively. (b) Transfer characteristic in push-pull gate voltage (in reference to the left gate).

Figure 1 (a) presents a micrograph of a fabricated BDT. It has six terminals: a grounded electron source (V_{SS}), left and right gates (V_{LG} and V_{RG}), and three biased drains (V_{TD}, V_{LD} and V_{RD}). The top drain is a pull-up terminal while the left and right drains are output terminals. In Fig. 1(b), dependence of I_{LD} and I_{RD} on voltage applied at the gates in push-pull bias fashion (V_{LG} = - V_{RG}) is shown. The voltages applied in the drains are: V_{LD} = V_{RD} = V_{TD} = 1 V. We observe that I_{LD} first increases as a function of gate voltage then decreases. This is due to the fact that the channel first is being pinched off, then, as the gate voltage is further increased, the electrons are steered from the right drain into the left drain, and, eventually, the channel pinches off again. At the peak between the steering region and the pinch-off region, we have maximum conductivity. Note that the pinch-off gate voltage is the point defined when current starts decreasing. The I_{RD} has the identical response, but is mirrored about the center axis. This positive and negative

transconductance g_m region characteristics, enables circuits that are inverting and non-inverting, depending only on gate offset voltage. The shape of this transfer characteristics makes it ideal for a frequency doubler. A gate bias that enables the input to swing past either side of the peak output current will result in an output signal that is twice the input frequency. A circuit utilizing this effect can have a significant gain.

Identical characterization as shown and discussed above was also performed for the BDT with the channel width of 300 nm and 80 nm gate-channel trench width.

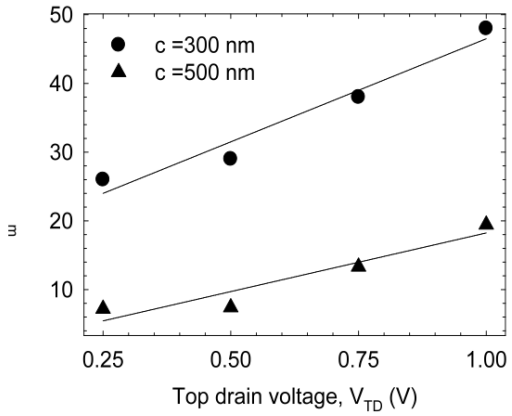


Fig. 2. Comparison of change in transconductance as a function of applied drain bias and a linear fit for BDT with c = 300 nm and 500 nm.

Figure 2 illustrates our major result, namely, the dependency of the transconductance g_m on the channel width c. We observe that for small devices, g_m is higher than the large devices. This is because of the fact that in small devices, the electric field effect produced by gates is strong enough to control and steer electrons along the channel due to its smaller trench width of 80 nm. On the other hand, in large devices, a trench width of 100 nm is too large for the gates to control the current transport efficiently. Since the channel is wider, the electric field effect of gates becomes weaker along the central part of the channel, which reduces the control of gate sweep. This, in turn, reduces the change in current with applied bias, which gives smaller g_m values.

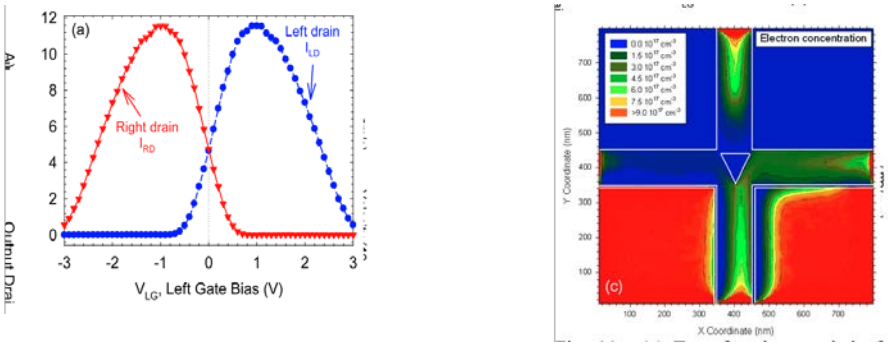


Fig. 3(a) MC simulated transfer characteristics for the 500-nm channel BDT of reference. The values corresponds to the x-axis are the left gate voltage ($V_{LG} = -V_{RG}$). (c) 2D map of the carrier concentration for V_{LG} = -0.3 V.

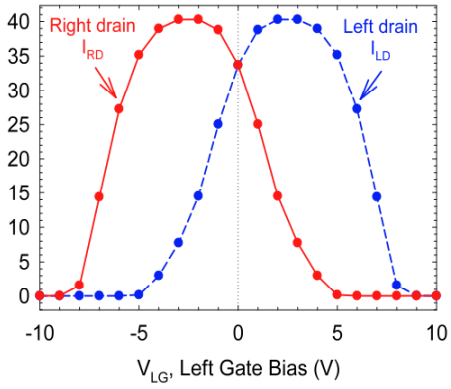


Fig. 4. Right and left drain currents as a function of left gate voltage, computed using the FEA simulation for the 300-nm channel BDT of reference.

Our experimental studies were directly compared to both Monte Carlo (MC) and finite element analysis (FEA) physical analysis in order to directly assess how accurate are our simulation tools. Figure 3 shows the MC results for both the transfer function and the underlying 2D field distribution, while Fig. 4 presents the same transfer function modeling, but using the FEA method. We note that in both cases the agreement between experiments and our modeling is very satisfactory.

(b) Experimental characterization of ballistic transport in TBJs fabricated out of 2EDG heterostructures. This thrust has been supervised by Profs. Sobolewski and Margala (co-PIs) and executed by the graduate students H. Irie. Additional assistance was provided by O. Magana (visitor).

We have completed our extensive experimental characterization of carrier transport dynamics in our nanostructured TBJs excited by picosecond electrical transients. Our measurements were performed using developed by us a femtosecond electro-optic (EO) sampling system. As a test sample, we used a TBJ rectifier consisting of two TBJs in parallel and placed in a coplanar waveguide (CPW). The subpicosecond electrical excitation pulses were generated by an optically triggered photoconductive switch, while a $LiTaO_3$-based EO transducer measured the waveform of the incident and transmitted voltage signals with a subpicosecond temporal resolution. We used the special "experiment-on-chip" configuration (see Fig. 5), which allowed the rectifier's electrical response to be studied with a bandwidth of up to 1 THz.

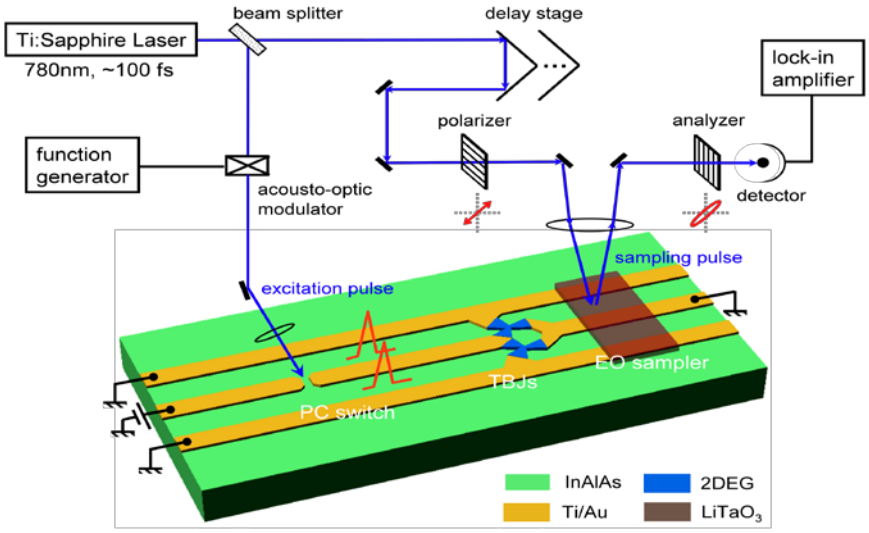


Fig. 5. Optics system and integrated device chip for the time-domain EO sampling measurement of a TBJ rectifier.

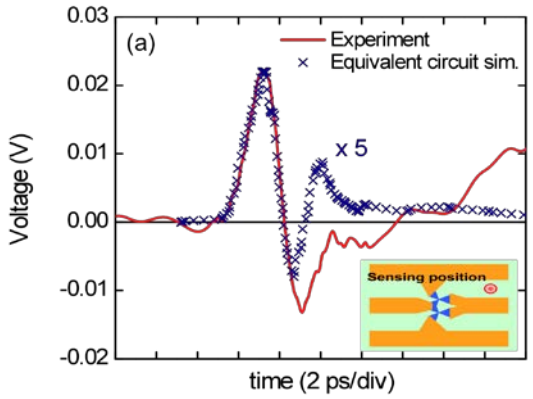
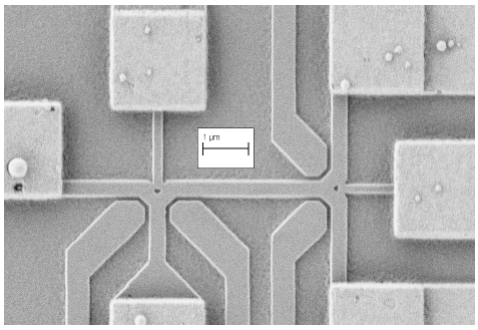


Fig. 6. Subpicosecond response of a TBJ rectifier (solid line) and circuit simulations (crosses). The inset shows EO sensing position with respect to the TBJ.

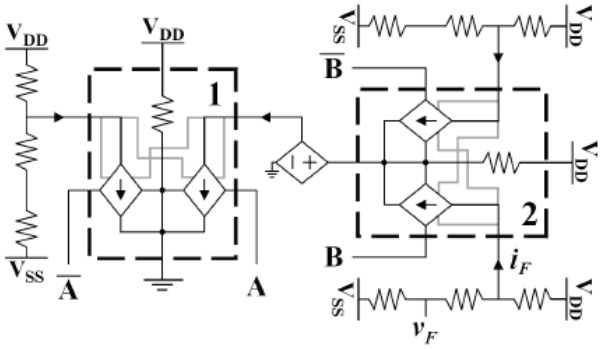
Figure 6 shows the subpicosecond TBJ response (solid line) collected after the nanostructure (inset in Fig. 6) and we observe an excellent agreement between the experiment and the equivalent-circuit-based simulation (crosses). From the Fourier transform of the time-domain signals, frequency spectra of incident and transmitted signals up to approximately 0.7 THz were successfully obtained. The TBJ rectifier did not degrade the frequency spectrum of the transmitted electrical pulses within the studied frequency range, which indirectly confirmed its high-frequency performance in THz frequencies. The limiting factor of the system bandwidth was studied. It was shown that the wave propagation properties of the CPW, rather than the intrinsic response of the PC switch, limited the system bandwidth. The intrinsic response of the PC switch had a subpicosecond FWHM and rise time that promises an extension of the bandwidth >1 THz by reducing the dispersion effect during the wave propagation.

(c) Circuit and systems aspects of ballistic electronics, including exhaustive simulation, analysis, and modeling of gate-level ballistic circuits. This thrust has been supervised by Profs Margala and Ampadu (co-PI) and executed by student D. Wolpert.

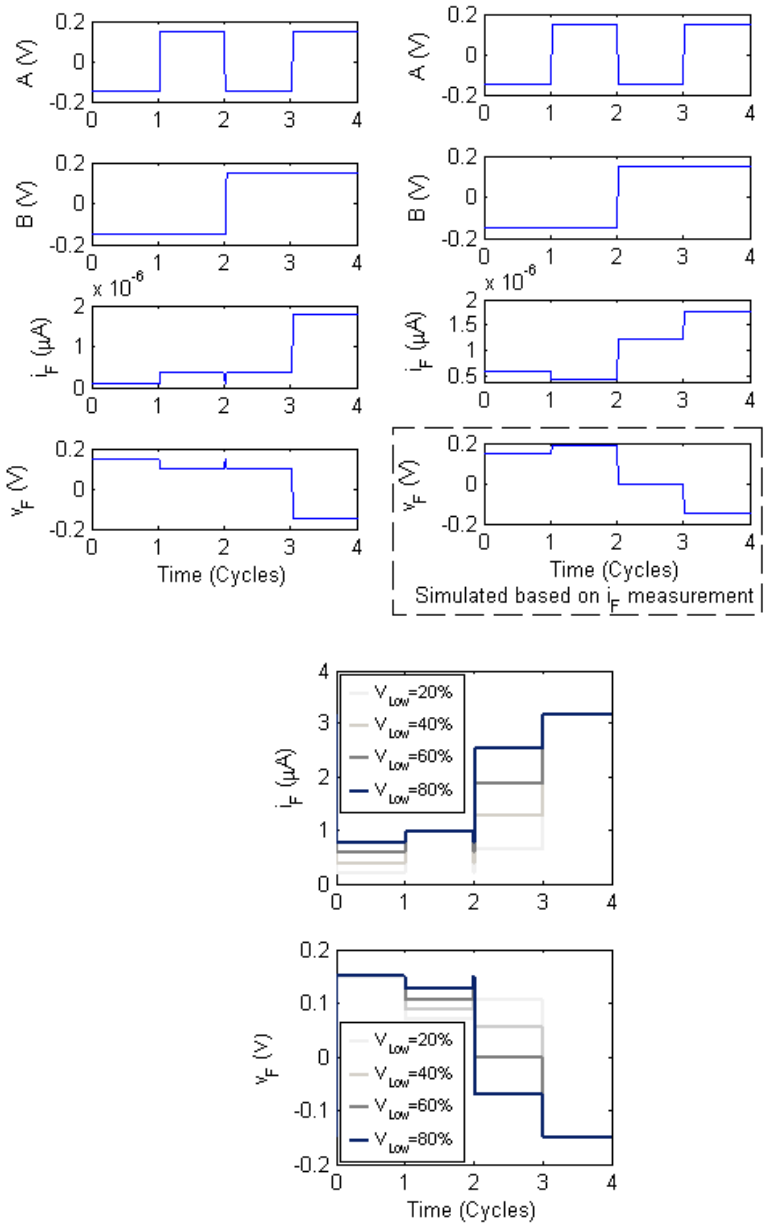
We have solved an apparent discrepancy between our measured NAND gate [Fig. 7(a)] response and the empirical NAND gate model consisting of two BDT device models connected in a drain-source configuration [Fig. 7(b). The discrepancy, shown in Fig. 7(c) and Fig. 7(d) for the i_F and v_F plots, arose because the empirical model did not consider the difference in drain potential between the left and right drains of the left BDT in Fig. 7(a). The left drain of that BDT is connected to a bias voltage, and the right drain of that BDT is the sum of the three bias voltages used to bias the right BDT. This difference between the drain biases causes the A = 0/B = 1 state output current to be skewed towards the A = 0/B = 0 state output current, shown in Fig. 7(d). To fix this issue with the model, we have included a new empirical data set in the current-controlled voltage sources (shown in Fig. 7(b) that includes the impact of each drain voltage in each BDT on that BDT's drain output. This results in the updated model shown in Fig. 7(e), which is shown to match the measured outputs much more closely (v_{Low} is a measure of the potential difference between the left and right drains in the left BDT).



(a)



(b)

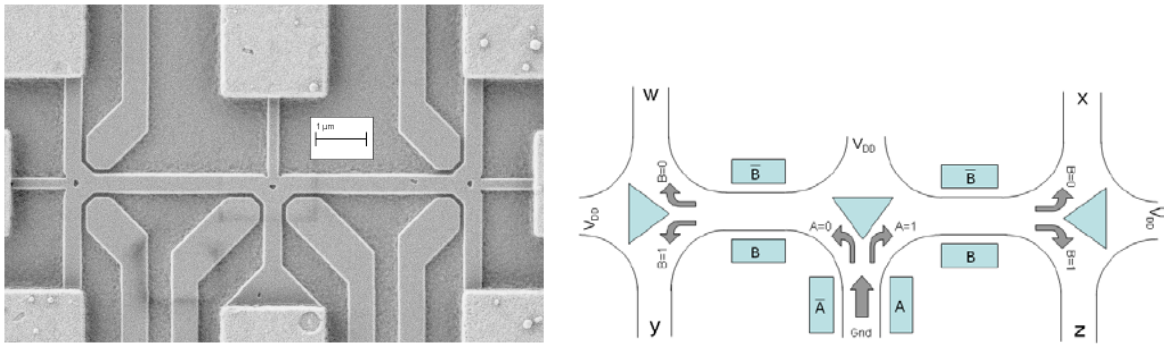


(c) (d) (e)

Fig. 7. (a) NAND gate SEM, (b) updated model, and waveforms from (c) previous model, (d) measured results, and (e) new model.

The GPG device has been fabricated and measured. An SEM of the fabricated gate is shown in Fig. 8(a), with a schematic of the gate operation shown in Fig. 8(b). Electrons enter the lower central channel, and are steered left or right by gate A. The electrons then can enter either the left or right drain of the central BDT, where they are further steered by the two gates controlled by the input B. Electrons are steered into the output terminal *W* when A = 0/B = 0, output terminal *X* when A = 1/B = 0, output terminal *Y* when A = 0/B = 1, and output terminal *Z* when A = 1/B = 1.

By connecting the output terminals appropriately to external nodes (e.g., *F* and *!F*, not shown), any two-input logic functionality can be created.



(a) (b)

Fig. 8. General purpose gate (a) SEM and (b) schematic.

The fabricated GPGs were measured at the Cornell CNF and the measurement results are shown in Fig. 9 for the XOR and XNOR GPG gate configurations (where terminals *W* and *Z* are connected together and terminals *X* and *Y* are connected together). The input pattern is shown in Fig. 9(a). The measured results in Fig. 9(b) indicate the correct XOR functionality with the A = 0/B = 1 and A = 1/B = 0 states resulting in logic high and the A = 0/B = 0 and A = 1/B = 1 states resulting in logic low. The measured results in Fig. 9(c) indicate the correct XNOR functionality, with the A = 0/B = 0 and A = 1/B = 1 states, resulting in logic high and the other two states resulting in logic low. This is the first demonstration of XOR and XNOR functionality with BDTs.

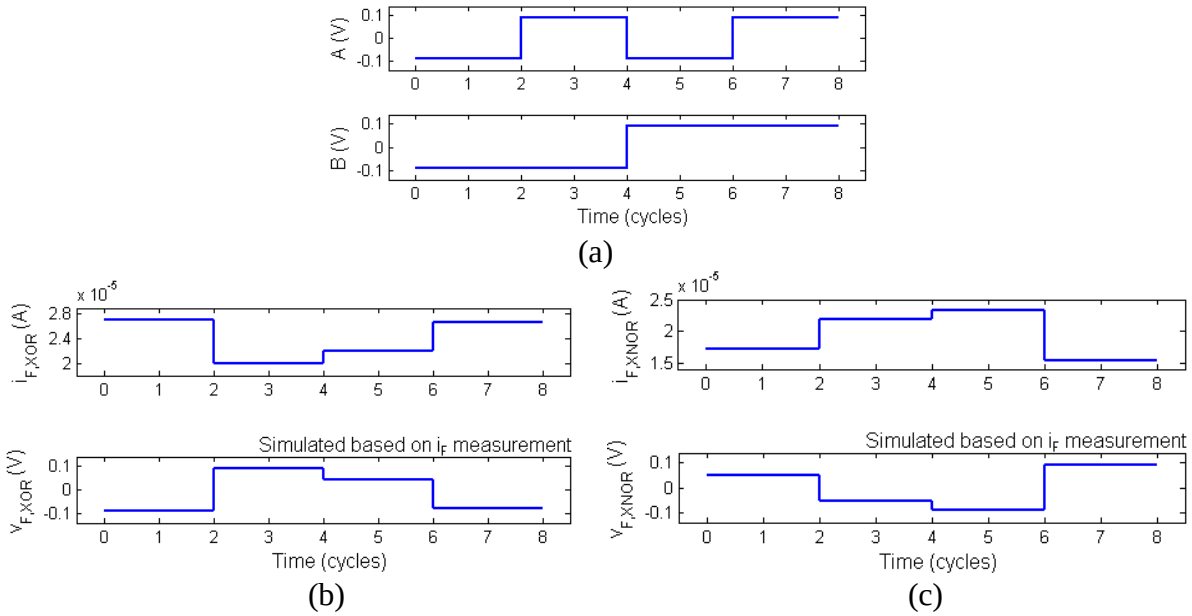
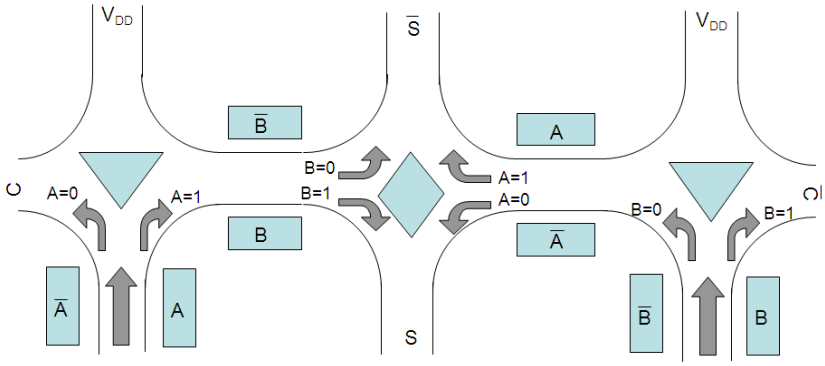
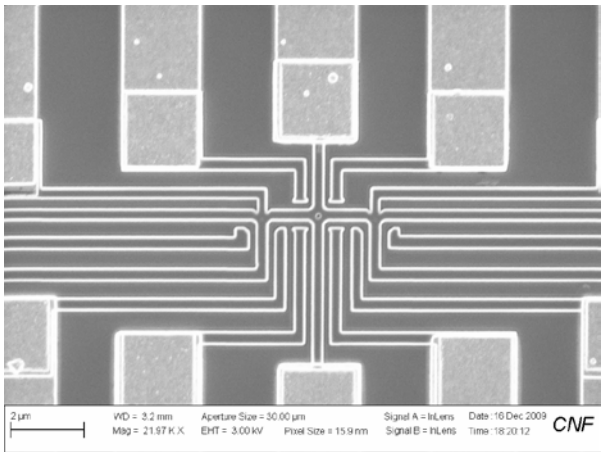


Fig. 9. Measured results from GPG. (a) Inputs, (b) XOR response, (c) XNOR response.

We have also designed and tested a half-adder based on three BDTs, as shown in Fig. 10. The half adder has two input entry channels, where electronics are injected into the device. The left and right transistors are regular BDTs. The middle transistor is a modified BDT, in which the center triangle is changed into a diamond so that electrons are allowed to exit through S and $\bar{S}$ terminals. When A = B = 1, a very limited flux of electrons from the right BDT is deflected to the center BDT; in contrast, most of the electrons injected through the left BDT are deflected to the center. Gate voltage on the connection between BDTs further steers the electron movement. Because of the high voltage on B, the electrons from the left BDT transfer to the terminal S, resulting in logic '0'. There are few electrons exiting from the terminal $\bar{S}$, resulting in logic '1'. The terminal C receives lower number of electrons than the terminal $\bar{C}$, resulting in logic '1' on carry. Similarly, if A = B = 0, the electrons contributed by the right BDT are deflected to the terminal S, resulting in logic '0'. There are more electrons exiting through C than through $\bar{C}$, resulting in logic '0' on carry. The functional correctness is examined in our Monte-Carlo simulator, and the results are shown in Fig. 11.

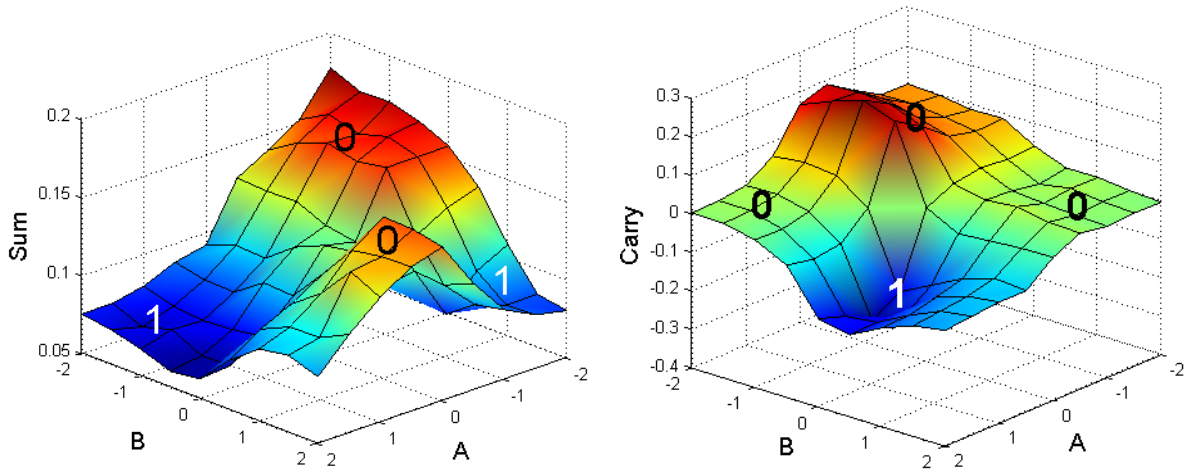


(a)



(b)

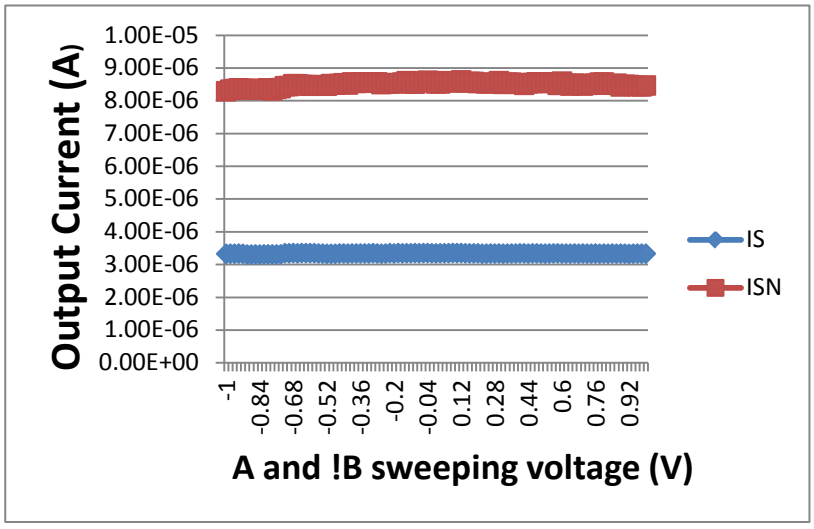
Fig. 10. Half adder design (a) schematic and (b) SEM image.



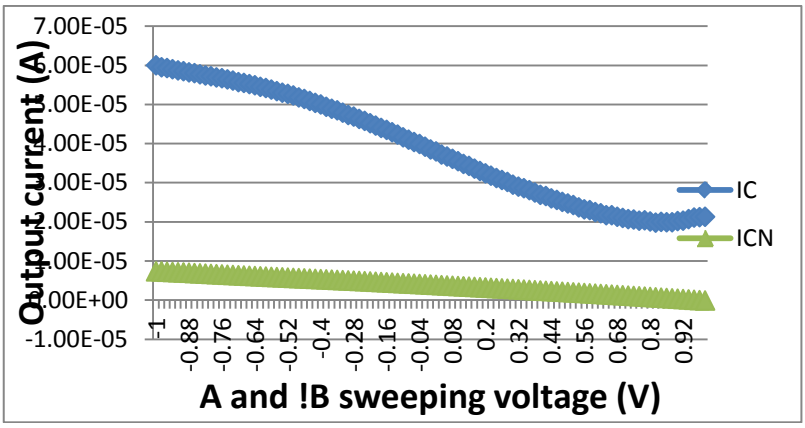
(a) (b)

Fig. 11. Monte-Carlo simulation results.

Measurement results based on the fabricated half adder [shown in Fig. 10(b)] were performed using a six-probe measurement station in the CNF at Cornell University. Because of the limitation of the measurement equipment, only a limited number of input combinations were examined on the proposed half adder. Fig. 12 shows the measurement results for the case input A! = input B. As shown, the voltage sweeping does not affect the output current of sum terminal, which conforms the functionality of the half adder. There is a 5-μA current difference between sum and sum_n; the trends for carry and carry_n are correct. Because of asymmetrical loads of pads, the current degradation for carry and carry_n is not equal as the sweeping voltage increases. In our interested operation voltage region (-0.2~0.2 V), we converted the measured current to voltage. As shown in Fig. 13, the output of sum and carry terminals are correct for the examined input cases, although the carry terminal has minor voltage fluctuation.



(a)



(b)

Fig. 12. Measurement results for (a) sum and (b) carry.

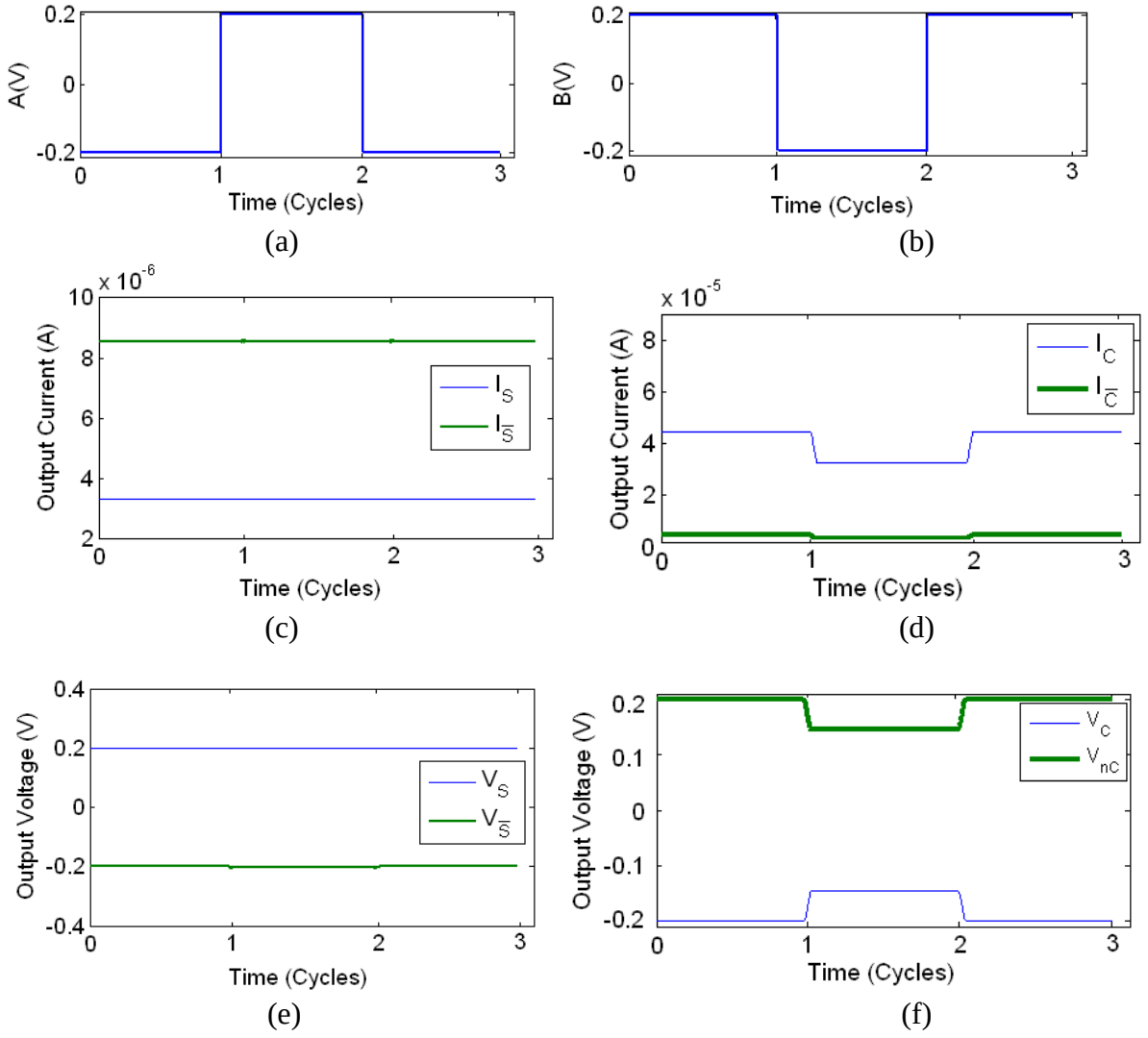


Fig. 13. Half adder function examination (a) input A waveform (b) input B waveform (c) sum current (d) carry current (e) converted sum voltage (f) converted carry voltage.

Presently, we have been looking ahead to use BDTs in large-scale circuits, integrating discrete BDT logic gates into cells consisting multiple of GPGs. To demonstrate the potential for large-scale integration, we intend to create a 5-GPG full adder. Circuit design with BDTs is going to be somewhat similar to traditional dual-rail logic design; each logic gate requires complimentary gate inputs. Unlike traditional logic design, the outputs *F* and *!F* will be generated by connecting the BDT drains to current-to-voltage converters, which then will produce the desired output .